Software-Oriented Memory-Management Design

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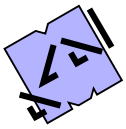
OUTLINE:

- **Motivation**
- **Architecture**
- **Evaluation**
- **Problems & Solutions**



ADVANCED COMPUTER ARCHITECTURE LAB

SOFTWARE ORIENTED MEMORY MANAGEMENT DESIGN

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Motivation

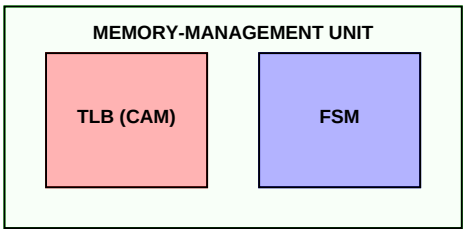
Trends in Microprocessor Design:

- **Faster clock speeds**
- **Larger and cheaper memories**
- **More on-chip devices**
- **Increased flexibility**
- **Increased focus on testability and reliability**

One Conclusion:

- **Make it SIMPLE**
- **Do it in SOFTWARE**

Implications for Memory Management?



Translation Lookaside Buffer

- **Large, fully associative, on critical path**

Finite State Machine

- **Good performance, limited flexibility**

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SOFTVM Design

VIRTUAL CACHE HIERARCHY
replaces
Translation Lookaside Buffer

CACHE-MISS INTERRUPT
replaces
Finite State Machine

Thesis tests validity
of software-oriented design
on memory management

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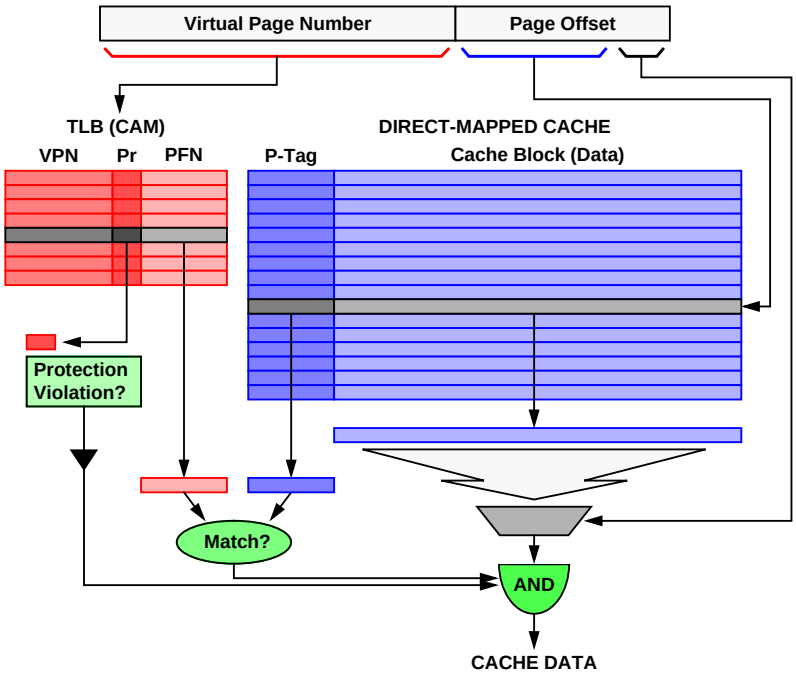
TLB Architecture



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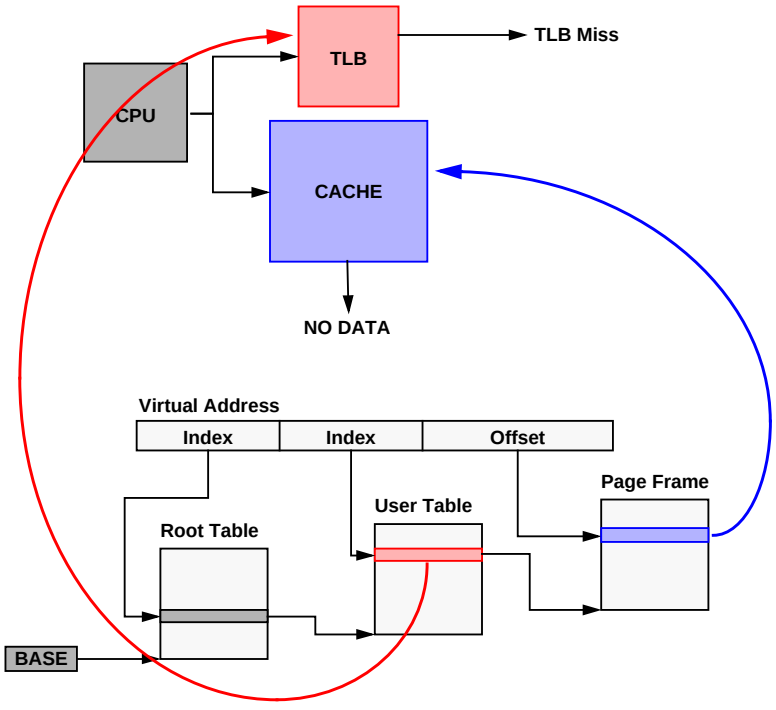
TLB Miss



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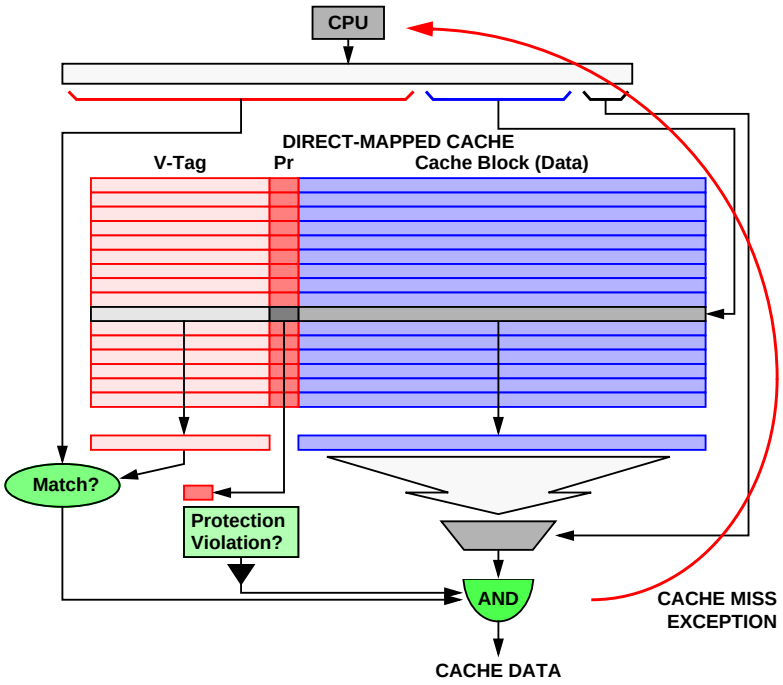
SOFTVM Architecture



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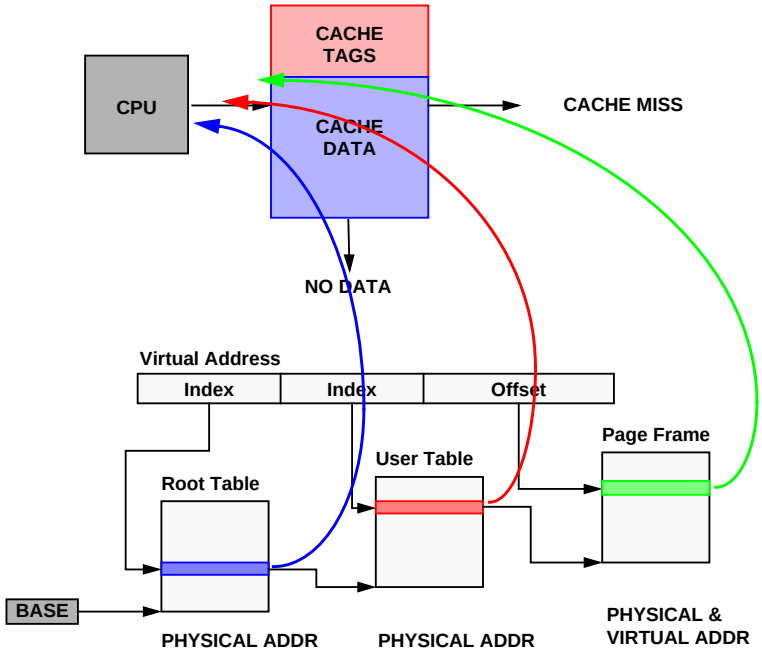
SOFTVM Cache Miss



Expectations

✔ **REDUCTION in DIE AREA**

✘ **SENSITIVE to CACHE ORGANIZATION**

✔ **MISSES INFREQUENT rel. to TLB**

✘ **MISSES EXPENSIVE rel. to TLB**

✔ **INCREASED FLEXIBILITY**

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Evaluation

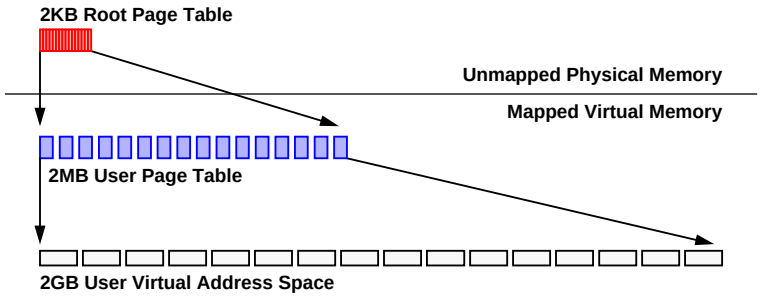
Simulated 5 Virtual Memory Designs:

- **SOFTVM - No TLB**
- **Ultrix/MIPS - SW-mgd TLB, part.**
- **Mach/MIPS - SW-mgd TLB, part.**
- **BSD/Intel - HW-mgd TLB, no part.**
- **PA-RISC - SW-mgd TLB, no part.**

TLBs: 128-entry I-TLB, 128-entry D-TLB
Fully associative, Random replacement,
16 entries in Protected Partition

Virtual cache hierarchies, Perfect memory

SOFTVM VM-simulation



Root-level handler: 20 inst, 1 PTE load

User-level handler: 10 inst, 1 PTE load

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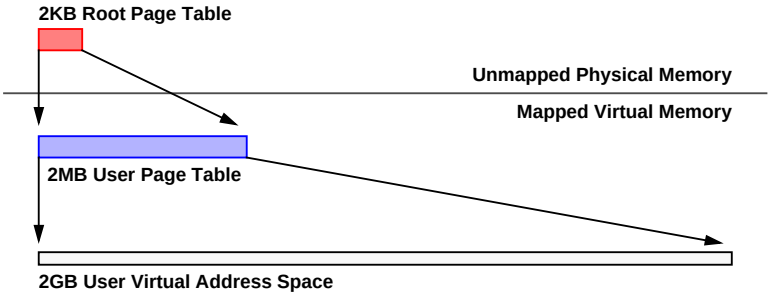
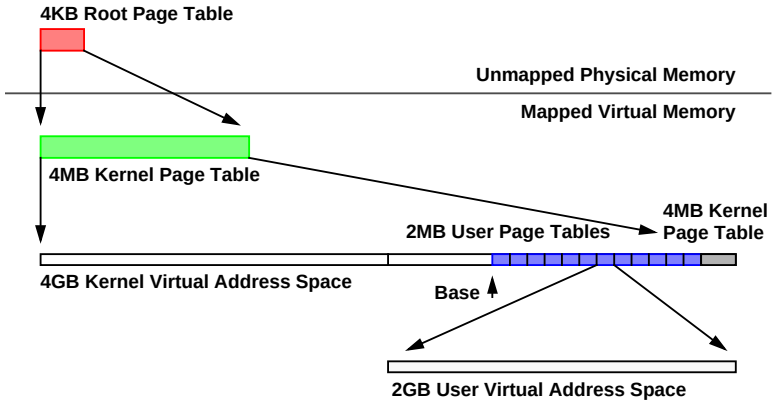
ULTRIX VM-simulation



Root-level handler: 20 inst, 1 PTE load

User-level handler: 10 inst, 1 PTE load

MACH VM-simulation



Root-level handler: 500 inst, 1 PTE load

Kernel-level handler: 20 inst, 1 PTE load

User-level handler: 10 inst, 1 PTE load

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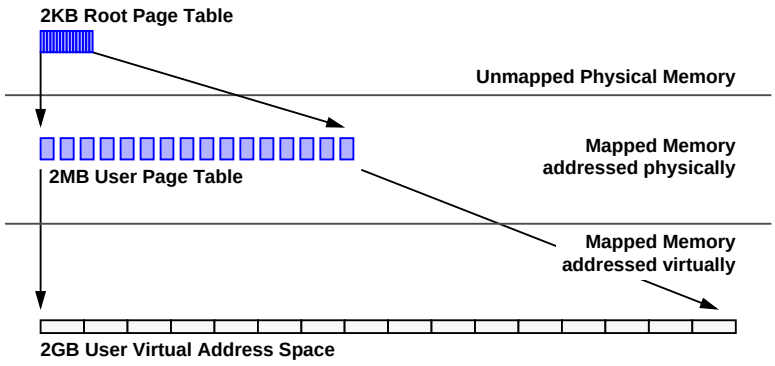
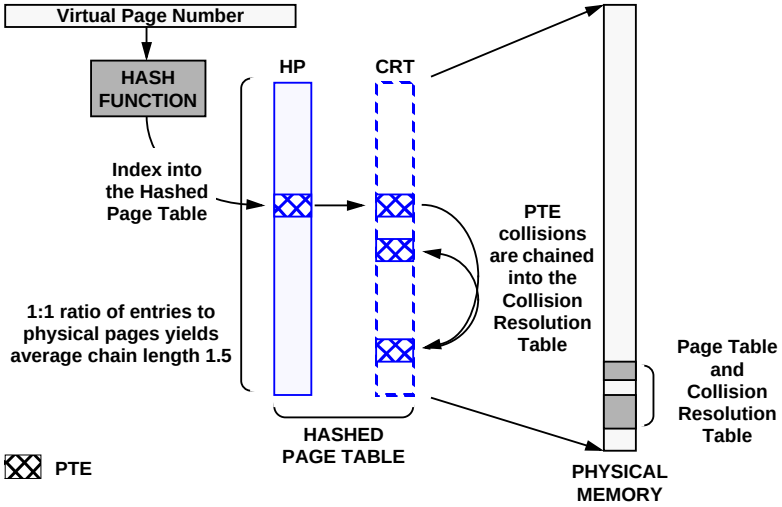
INTEL VM-simulation



User-level handler: 7 cycles, 2 PTE loads

PARISC VM-simulation



User-level handler: 20 inst, ≥ 1 PTE loads

PTEs are 2x size of other tables

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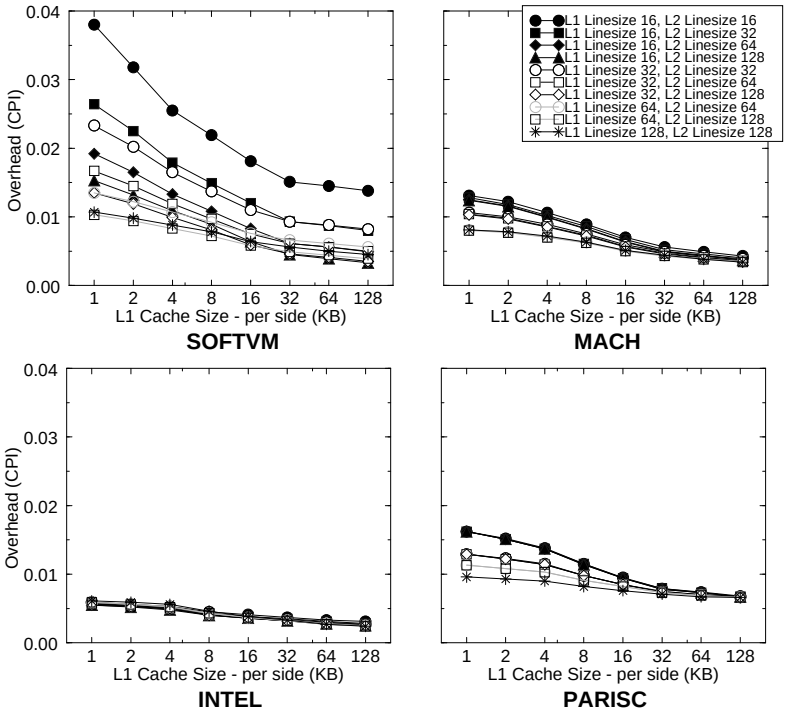
VM Performance: GCC



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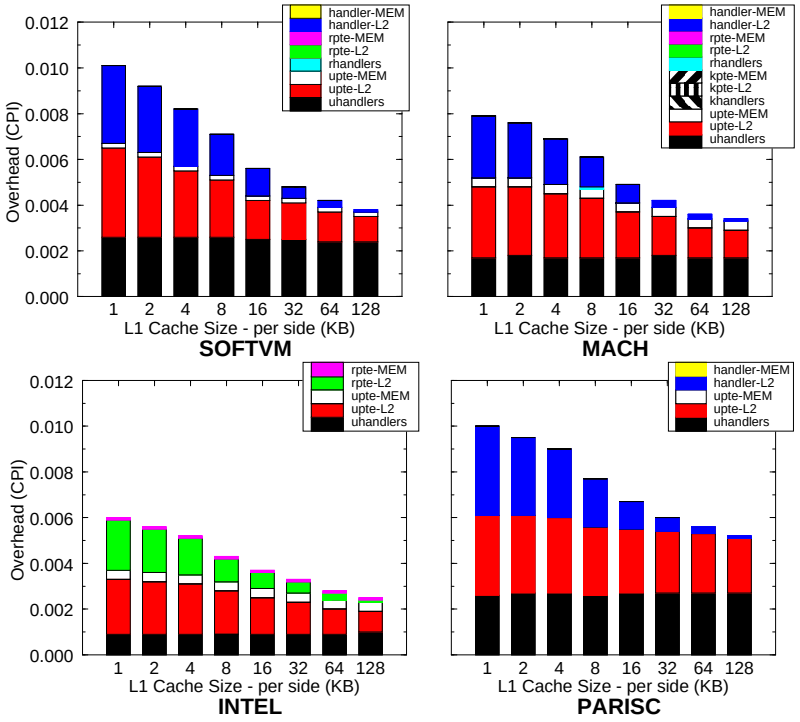
VM Break-downs: GCC



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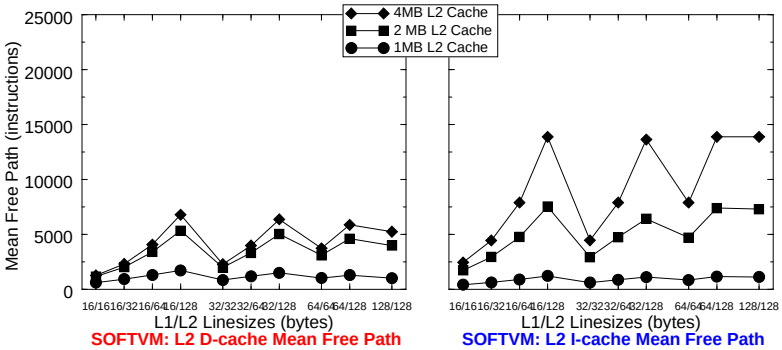
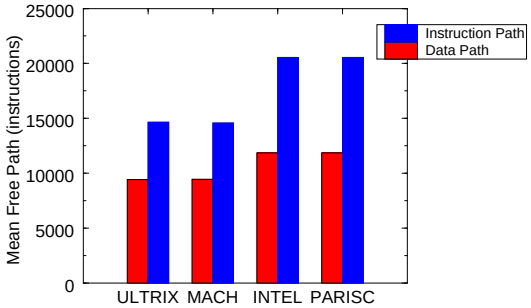
How Often: GCC





Hardware schemes: Mean time between TLB misses

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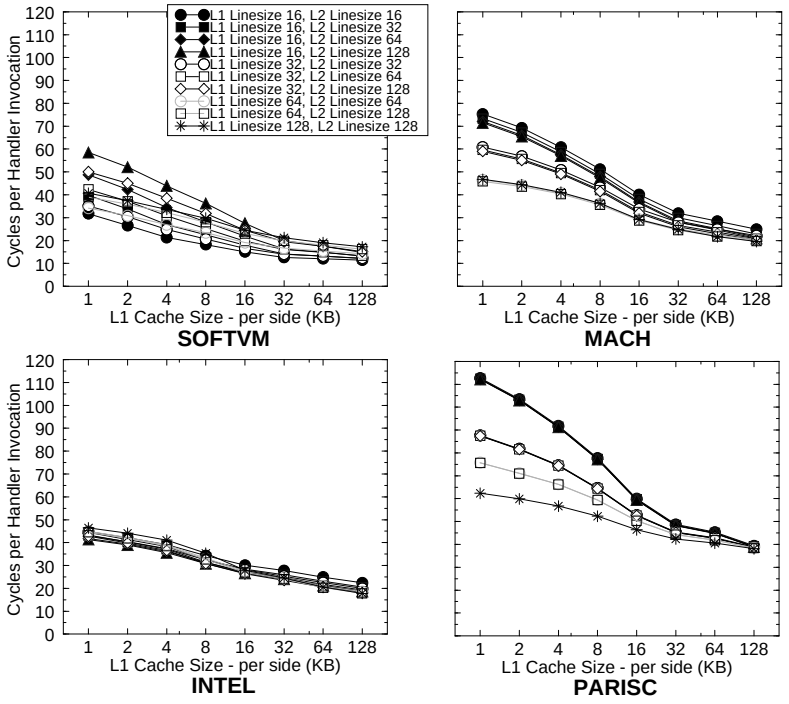
How Much: GCC



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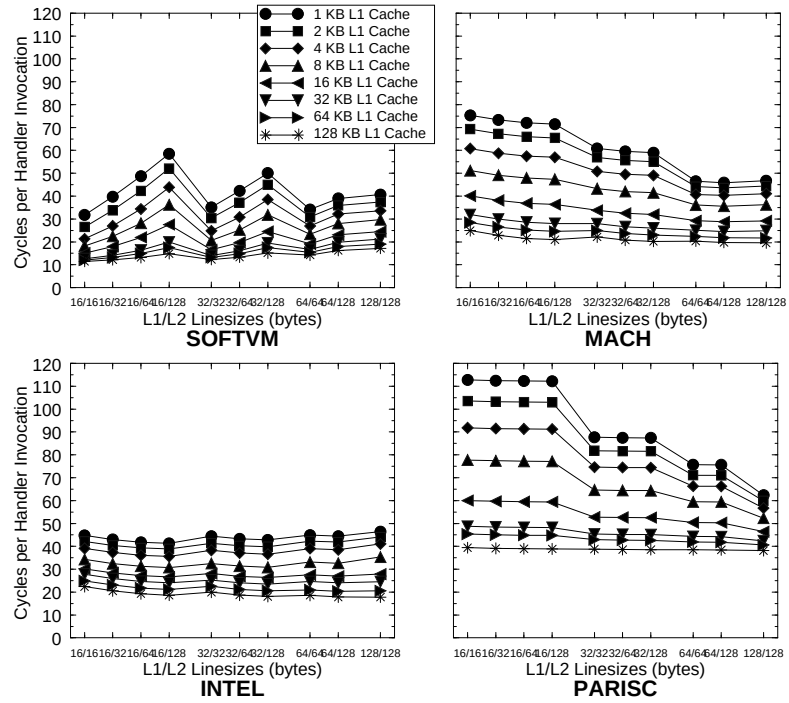
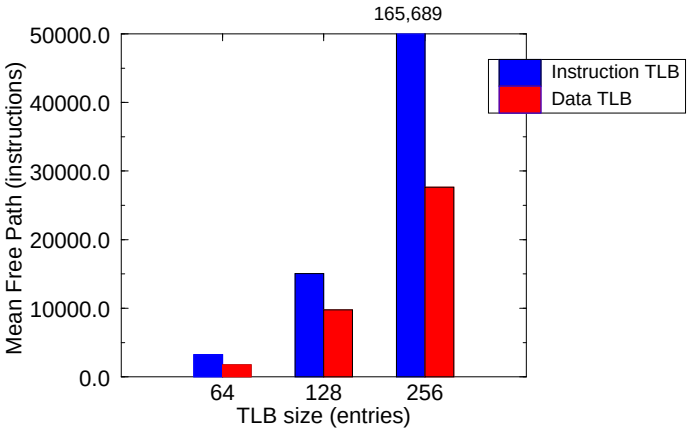
How Much: GCC



TLB Sensitivity: GCC



Mean free path of GCC — ULTRIX page table, 4MB caches

Hardware schemes VERY sensitive to TLB miss-rate ... Software scheme would look 5x better against 64-entry TLBs

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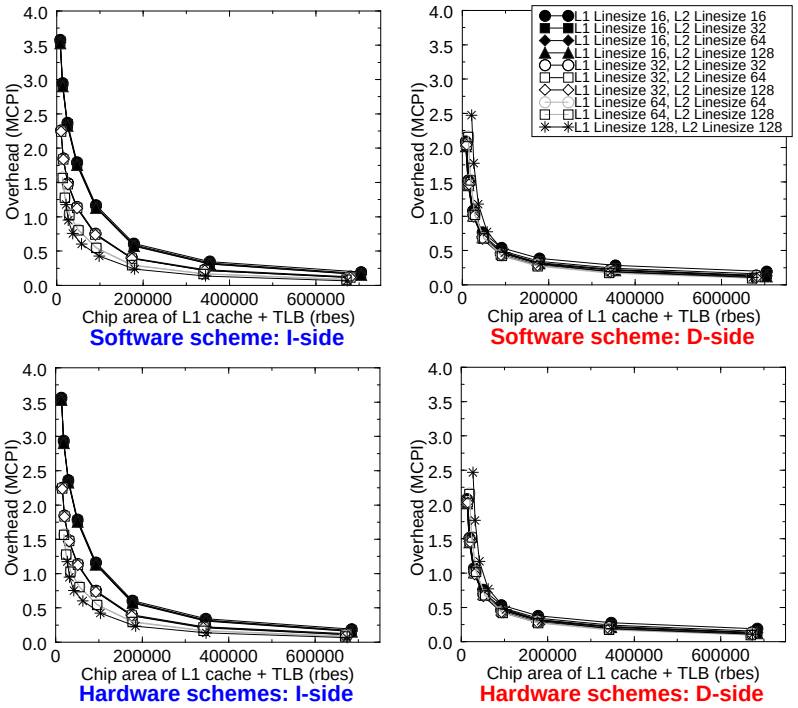
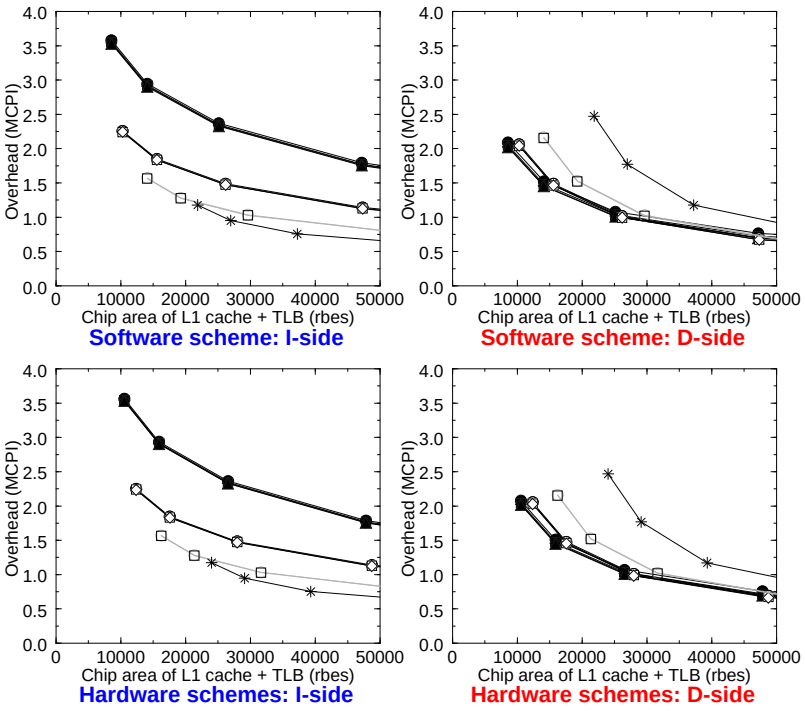
Bottom Line: GCC



Bottom Line (closeup): GCC



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Problems & Solutions ...

USE OF EXCEPTION MECHANISM

Exception Problem

CACHE-BOUND PERFORMANCE

Multimedia Problem

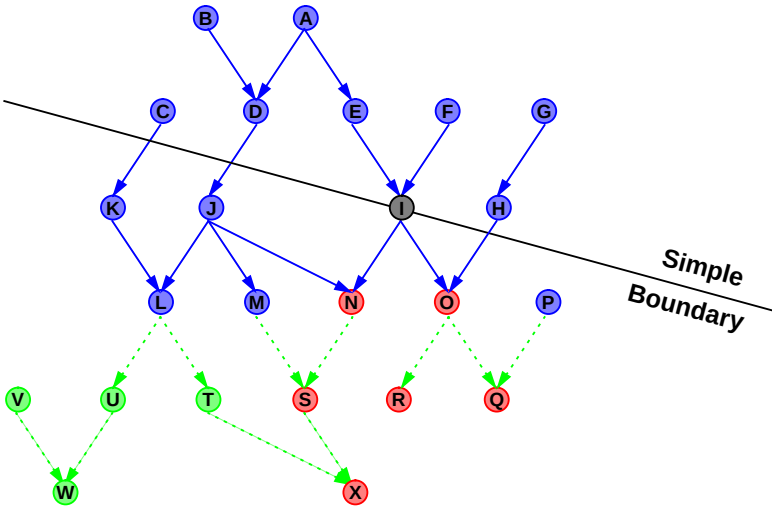
LARGE VIRTUAL CACHES

Synonym Problem

LEVEL-2 CACHES

Cost Problem

Exception Problem



Cost of Interrupt =
Cost of flushing Reorder Buffer

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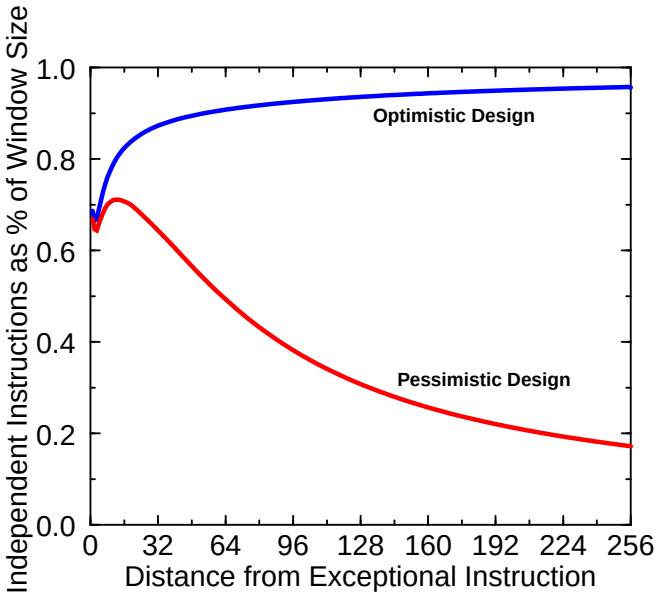
Potential Gains



Re-Execute Buffer

ROB Entry contains DEPENDENCY INFO

On Interrupt, DO NOT Flush Reorder Buffer

At Instruction Commit:

- **If DONE, Commit**
- **If waiting for EXECUTE, Wait**
- **If waiting for OPERAND, Re-Execute**

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ROB/REB Illustration

Detection of Exception

Reorder Buffer Inst	Dep's	Re-Ex Buffer
A	-	-
B	-	-
C	A, B	-
D	A, D	-
E*	C	
F	D, E	
G	D	
H	G	

Inst E at Head of ROB

Reorder Buffer Inst	Dep's	Re-Ex Buffer
E*	-	E: -
F	D, E	-
G	D	-
H	G	-
x1	-	
x2	x1	
x3	x2	
x4	x3	

Handler at Head of ROB

Reorder Buffer Inst	Dep's	Re-Ex Buffer
x1	-	E: -
x2	x1	F: D,E
x3	x2	next: I
x4	x3	-
x5	x4	
x6	x5	
x7	x6	
x8	x7	

Re-Execution of E & F

Reorder Buffer Inst	Dep's	Re-Ex Buffer
xW	xV	-
xX	xW	-
xY	xX	-
xZ	xY	-
E	-	
F	D, E	
I	-	
J	I	

Multimedia Problem STREAM

MULTIMEDIA HAS NO TEMPORAL LOCALITY

WORST-CASE SCENARIO:

Take an exception for every cache line

SOLUTIONS:

- **Prefetch buffers**
- **Prefetch into L2 cache**
- **Provide unmapped regions to user**

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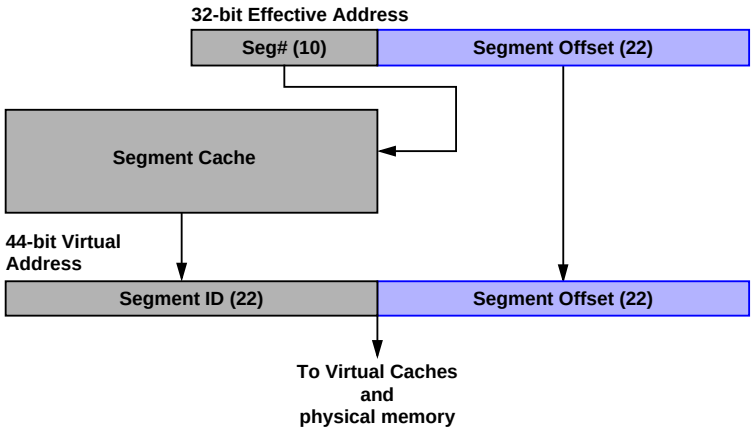
Unmapped 4MB Superpages



Alternative (Non-Segmented) Solution:

- **Small Superpage TLB (BAT Registers)**

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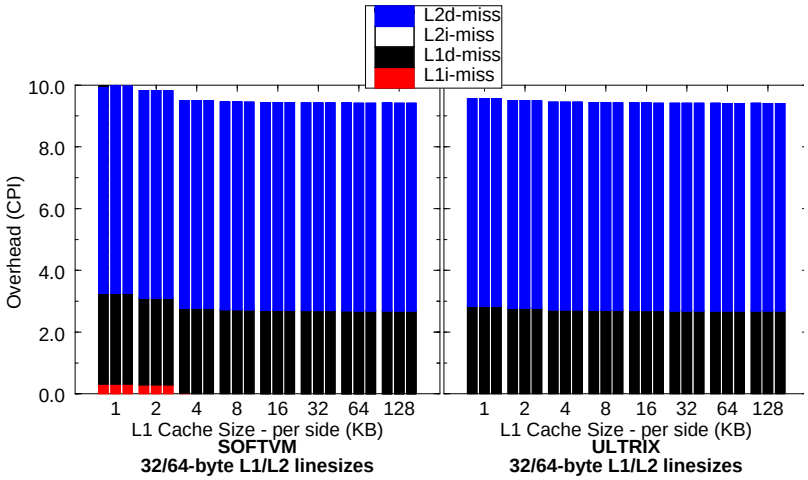
STREAM Performance



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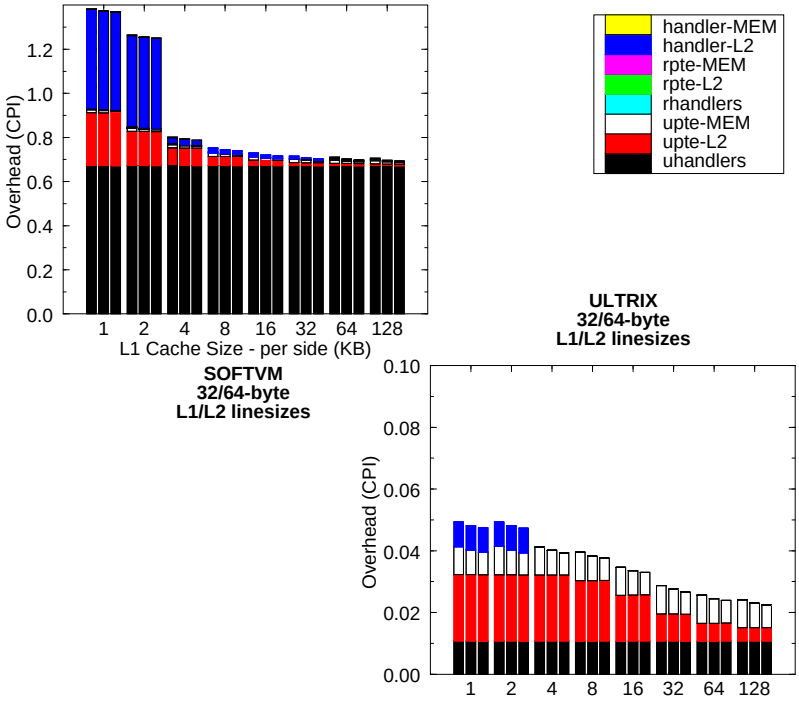
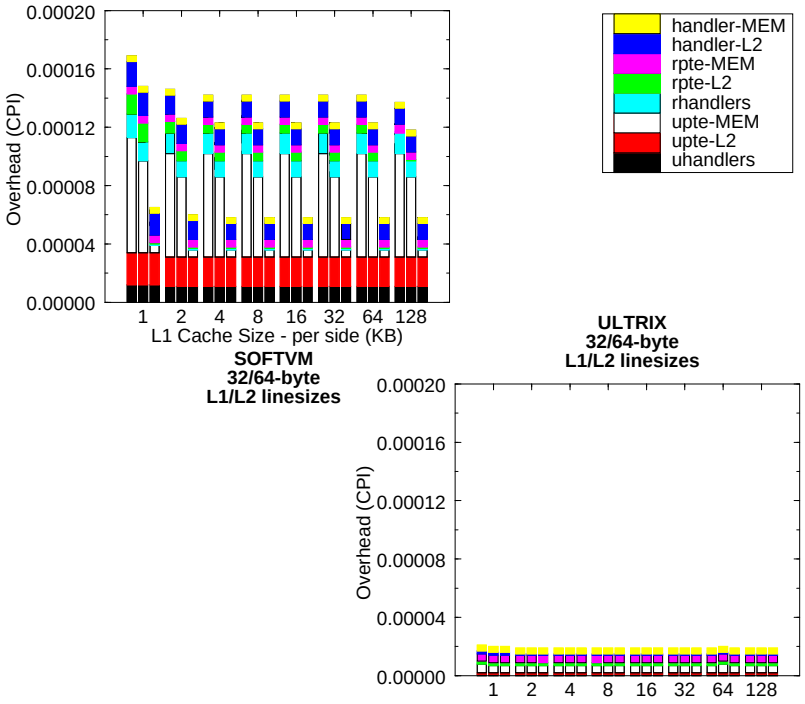
STREAM VM Performance



... with Superpages



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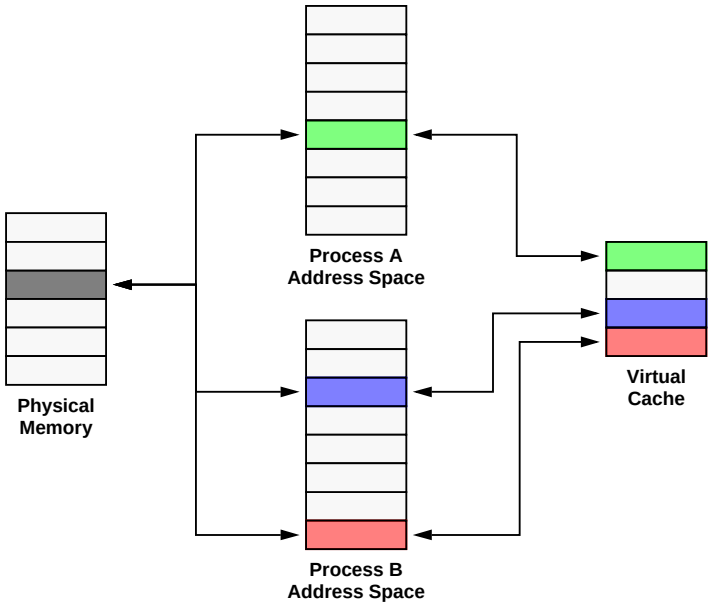
Virtual Cache Synonym Problem



Solutions to Synonym Problem

HARDWARE

- Backpointers

SOFTWARE

- OS/2: Eliminate Aliasing
- SunOS: Aliases map to same cache line
- SASOS: Eliminate Aliasing

HARDWARE/SOFTWARE

- Segmentation ....

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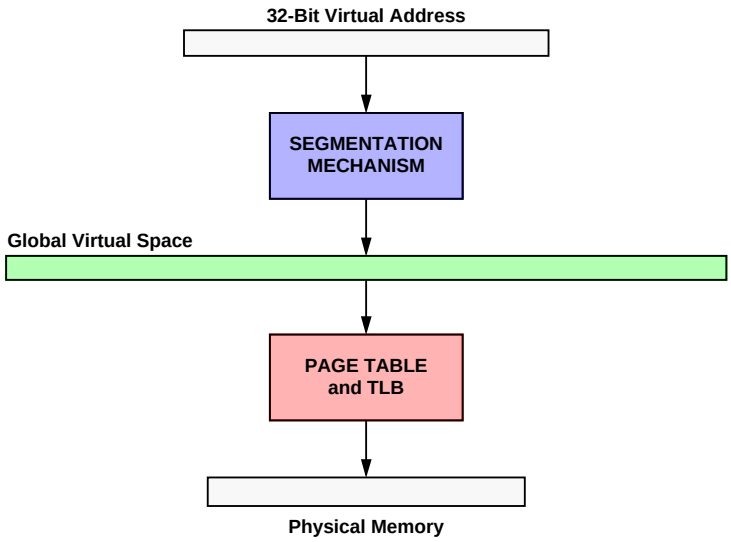
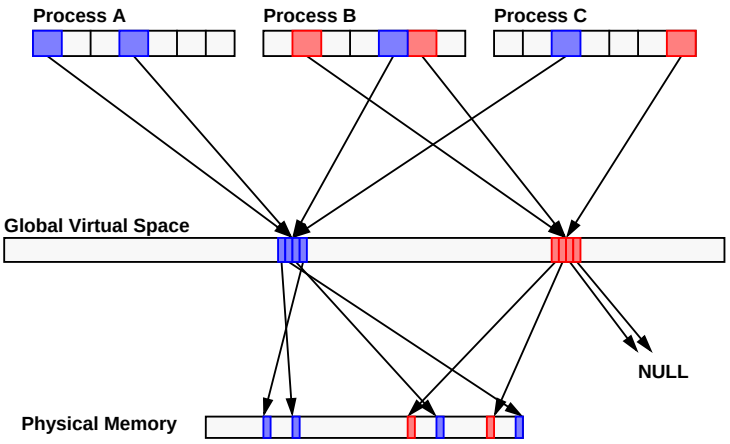
Segmentation



Segmented Solution

ALIASING without SYNONYM PROBLEMS



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Cost Problem

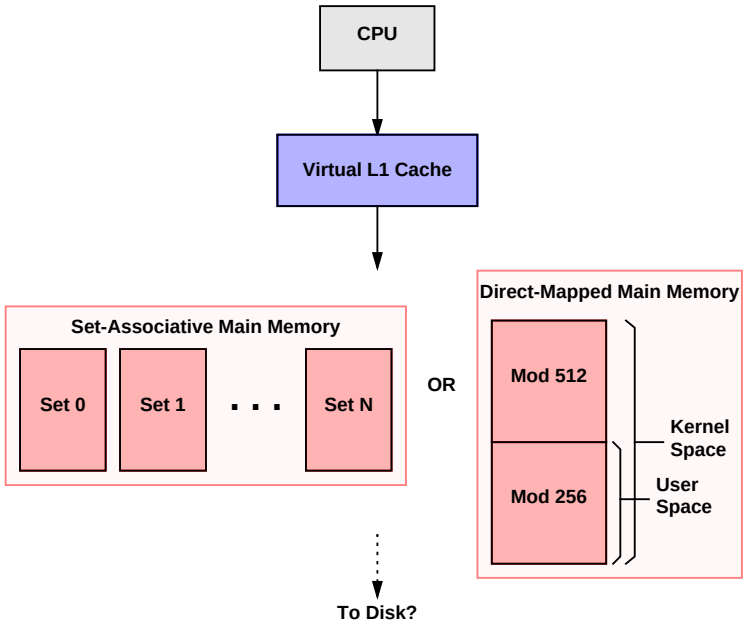
Solution Requires (LARGE) L2 Caches

What about embedded market?
What about cost-cutter market?

Implement L2 Caches in DRAM,
Call it MAIN MEMORY

Requirement: ability to
pin down critical regions ...

Virtually-Addressed Main Memory



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Conclusions

Elimination of MMU is Possible

Cycle Time can DECREASE

Performance can INCREASE

Software-Managed: FLEXIBILITY

Examples of Usefulness:

- **Shared-Memory Multiprocessor**
- **Real-Time Processing**
- **Architecture Emulation**
- **Restricted Reconfigurable Computing**