Radio Frequency Effects on the Clock Networks of Digital Circuits

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Abstract — **Radio frequency interference (RFI) can have adverse effects on commercial electronics. Current properties of high performance integrated circuits (ICs), such as very small feature sizes, high clock frequencies, and reduced voltage levels, increase the susceptibility of these circuits to RFI, causing them to be more prone to smaller interference levels. Also, recent developments of mobile devices and wireless networks create a hostile electromagnetic environment for ICs. Therefore, it is important to measure the susceptibility of ICs to RFI. In this study, we investigate the susceptibility levels to RFI of the clock network of a basic digital building block. Our experimental setup is designed to couple a pulse modulated RF signal using the pin direct injection method. The device under test is an 8-bit ripple counter, designed and fabricated using AMI 0.5 μm process technology. Our experiments showed that relatively low levels of RFI (e.g., 16.8 dBm with carrier frequency of 1 GHz) could adversely affect the normal functioning of the device under test.**

Keywords: RFI, Pin direct injection method, Power reflection coefficient, Pulsed modulated RF, Clock network

I. INTRODUCTION

Current high performance integrated circuits (ICs), such as microprocessors, have very small feature sizes (e.g., 0.13 μm) and are clocked at frequencies well into the GHz range while operating at reduced voltage levels (e.g., 1.5 V). Although this has improved the ability and performance of modern systems, it has also increased their susceptibility to radio frequency interference (RFI). The electrical charge required in transistor switching decreases with relatively smaller IC feature sizes. Correspondingly, the energy required to disturb the switching process is reduced, making it easier to disturb the circuit with lower RFI signal levels. As the switching speed of the ICs increases and the supply voltage scales down, the noise margin also becomes smaller. This allows external disturbances, such as those induced by RFI, to degrade the signal integrity. Consequently, the electronic systems that are integrated with these high performance chips are more prone to be affected by lower RFI levels.

Numerous structures in a computer system (e.g., external wires, cables, PCB traces, bonding interconnects, internal metal chip signals like power, ground, and data lines) can act as antennae in the presence of RFI, which is either radiated from powerful radio transmitters, wireless network devices, mobile phones and PDAs, or intentionally generated for malicious reasons. These unintentional antennae can serve to couple RF noise into the core circuit [1, 2, 3]. RFI that is coupled by the system can induce unwanted currents, which cause various disturbances. The inherent non-linear behavior of electronic devices in digital circuits can also cause RF signal rectification and amplification and is said to be the primary upset mechanism for integrated circuits under RFI [4]. Also, inter-modulation, cross-modulation and other disturbances are immediate effects of interference [5]. These unwanted interferences, when interpreted as or superimposed on system signals, can cause spurious state changes on logic devices and system-level breakdown [3, 4].

The power levels and frequency range for which circuits are more susceptible to RFI have been studied recently. Previous studies observed changes on the I-V characteristics of diodes, BJTs, and MOSFETs under RFI [1]. Susceptibility levels of a microcontroller and a DSP chip have been measured for RF interference up to 400 MHz, and data corruption was observed on the communication path between the microcontroller and RAM memory [2]. The same study showed that 20 dBm RF interferences at 350 MHz were enough to trigger the reset pin of a voltage regulator. Another study investigated the effects of RF interference on the input ports of a 0.7 μm CMOS inverter with frequencies in the 20 MHz – 1 GHz ranges and power levels up to 15 dBm [3]. Dynamic failures in the form of variations in input pad propagation delay and static failures were observed when pad output signals were misinterpreted as they strayed beyond the high and low voltage logic thresholds. Hence, there is a growing concern over the electromagnetic compatibility of ICs in hostile RFI environments and wider RF frequency ranges, such as those at and above 1 GHz. To this end, power levels and frequency ranges of RFI to which high

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speed ICs are more sensitive, have been studied in this paper. Also, the input characteristics of the circuit, such as input impedance, are being investigated.

This work follows a system-level approach to quantify and generalize the susceptibility levels of digital ICs. On the system-level, signals in the basic blocks of memory and CPU are mainly composed of the clock, power-ground, and data networks. These signals are interpreted differently under normal operation. The timing and voltage levels of the data input/output signals are important, whereas for clock signals, the timing of low-to-high or high-to-low transitions is most critical. Any level shifts on power/ground planes can also cause malfunctioning of the circuit. In this study, we focused on measuring the susceptibility levels of the clock network. Our susceptibility test bench is designed to couple pulse-modulated RF signals on the clock network using the pin direct injection method to have better control of the power level that is applied to the device under test (DUT).

II. EXPERIMENTAL SETUP AND MEASUREMENT

The experimental setup is shown in Fig. 1. The 20 dB coupler is used to measure the power that is delivered to the circuit and the reflected power. High and low pass filters are used to eliminate the possible loading effect caused by a regular bias T. A 500 MHz high pass filter (HPF) is used to match the RF frequency, and the 100 MHz low pass filter (LPF) is used to match the RF envelope, which depends on the RF pulse frequency. Bypass capacitors are also used in the experimental setup to provide return current paths closer to the source current, thereby reducing loop area since less loop area means less radiation. A 12.5 dB RF amplifier is employed in this setup, and the bias voltage is set to zero at the initial test measurement.

The DUT in this study is an 8-bit ripple counter. The layout of the chip is shown in Fig. 2. It is designed and fabricated using the AMI 0.5μm process technology through MOSIS. The operating clock of the ripple counter is driven by a multiplexer that chooses between an internally generated clock and an external clock, an input signal to the circuit, "EXTCLK". A separate input signal, "CLKSEL" is used as a control signal to the multiplexer. In this study, we injected pulse-modulated RF signals into the EXTCLK input pin, observed the effect on the ripple-counter output, and recorded the required RF frequency and power level to trigger the output state change.

In the normal circuit operation, the ripple counter counts according to the internal clock of the chip, which is 11 MHz. Once we ensured the chip was working properly using the internal clock, we injected a pulse-modulated RF signal with pulse width of 10 μsec and 1 msec pulse period into the EXTCLK input pin of the chip. The reason for using pulsed RF instead of continuous wave is because the total energy of a pulsed RF signal is adjustable. When RF pulses are applied with a relatively low duty cycle, one percent in the setup, the total energy is much lower compared to continuous wave RF signals. This prevents the circuit from overheating and potential damage to RF signal generator and RF amplifiers caused by the reflected power. As we described earlier in the paper, the purpose of this study is first, to find out if, given a certain frequency, the circuit input impedance is constant; and second, to investigate the power level and frequency range to which the counter is most sensitive — i.e., those frequencies and power levels that cause output state changes. Following the experimental setup in Fig. 1, with 20 dB coupler applied, we measured the reflected and delivered power at each port of the coupler at frequency range from 1.0 GHz to 1.3 GHz, above which there are no obvious state changes observed with the 12.5 dB RF amplifier employed (because the safe range that guarantees the correct functioning of the RF amplifier requires that the power level applied is below 10 dBm), and below which is out of the scope our current concern in this experiment.

First, we measure the reflected and injected power, with power loss taken into account. Since the input impedance is a function of reflection coefficient, we varied the injected power from 0 to 25 dBm with one dBm per step, reiterating the process with RF frequency at 1.0 GHz, 1.1 GHz, 1.2 GHz, and 1.3 GHz, to observe if this produced a constant power-reflection coefficient. Then, the power levels required to cause state changes at each of these carrier frequencies were measured.

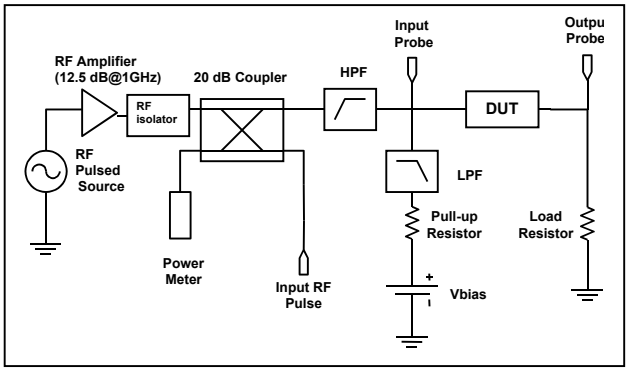


Figure 1. RF Injection Experiment Setup

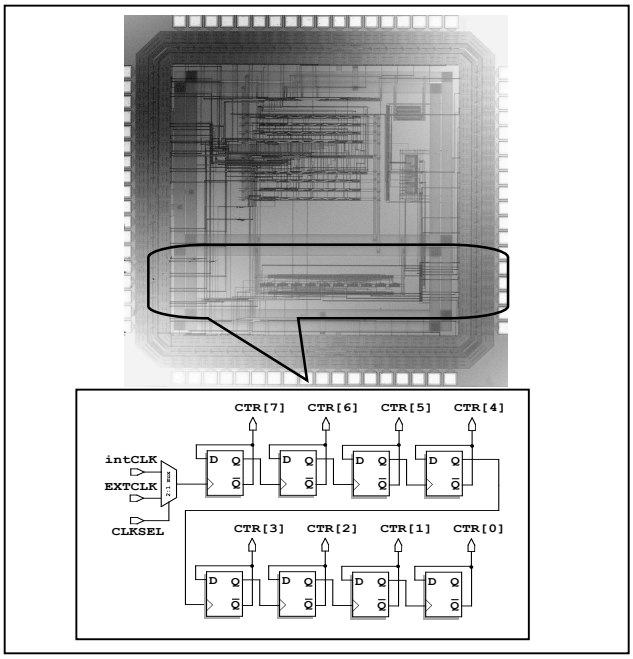


Figure 2. Die photo of the DUT and schematic of the 8-bit ripple counter

III. EXPERIMENTAL RESULTS AND ANALYSIS

For different frequency and power levels of the injected RF signal, we observed the least significant bit of the ripple counter output, CTR [0] in Fig. 2. When RF pulses are coupled into the input EXTCLK pin of the counter, we noticed clear state changes at the output, as shown in Fig. 4(c), for a source frequency of 1.0 GHz.

Table 1 summarizes the required RF power levels to make state changes. P_{IN} stands for power injected; the reflected power because of the impedance mismatching is called P_R; and the power that is actually delivered into the pin is named P_D. The latter is derived from P_{IN}, and P_R. This table also includes the power-reflection coefficient Γ, which is defined as square root of the reflected power P_R, versus power injected P_{IN}, and its relationship with power delivered, P_{IN} is shown in Fig. 3.

From Fig. 3 and Table 1, we observe that the input impedance of the counter circuit is frequency-dependent; this is because of the unmatched load and standing waves. However, this impedance is independent of the injected RF power with the power level we applied, within which the input device is operating in the linear region. At the frequency at which the circuit is more susceptible (i.e., the one at which less power is required to make a state change, 1.2 GHz in this case), the power-reflection coefficient is the lowest. At this frequency the power coefficient is less than half than those at other frequency ranges. This may be caused by the input circuitry resonant frequencies, which are around 1.2 GHz.

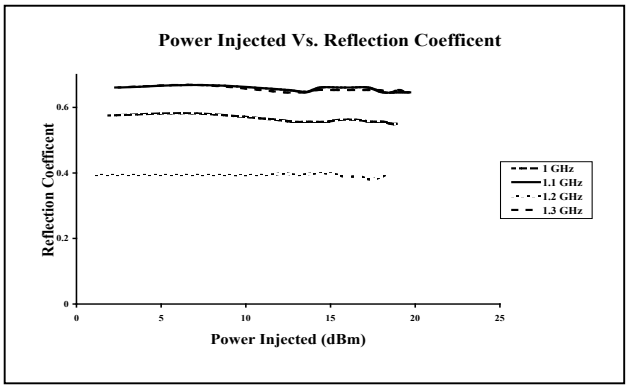
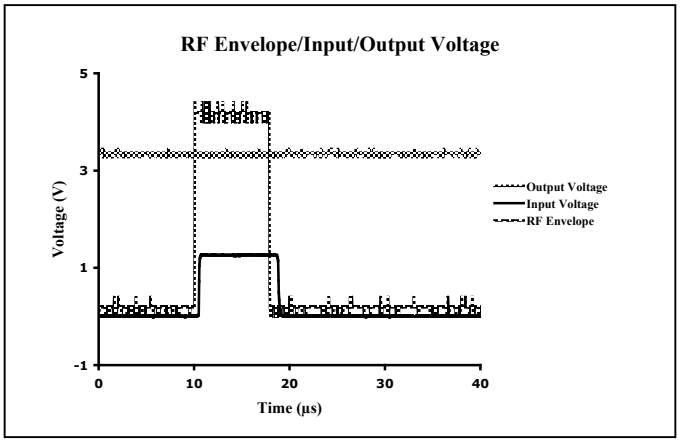


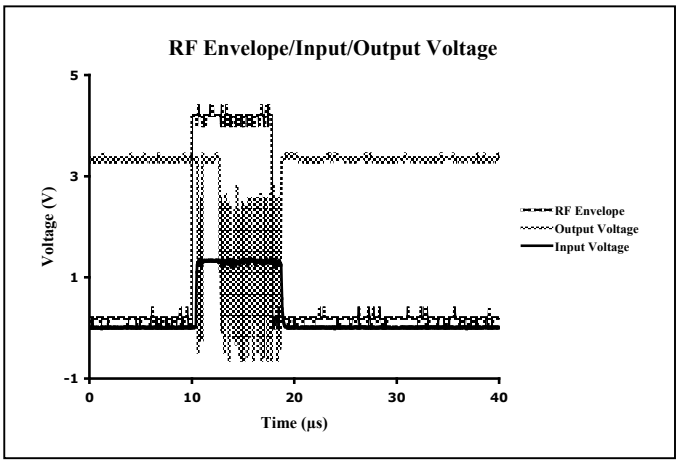
Figure 3. Power-reflection coefficient

Table 1. Power required making state changes

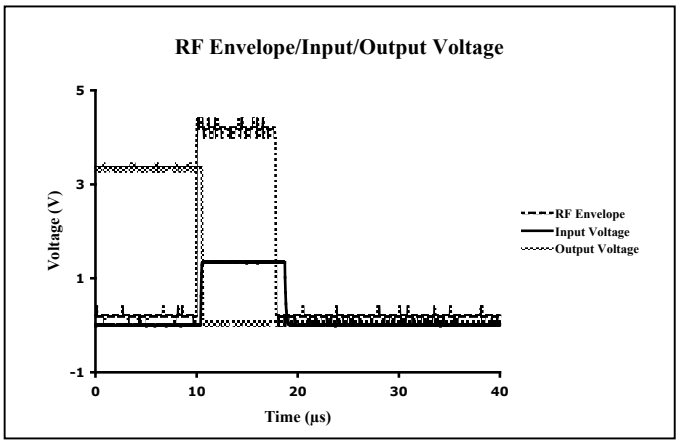
Freq (GHz) Power (dBm)	1.0	1.1	1.2	1.3
P_{IN}	20.1	17.9	16.9	20.5
P_R	13.3	13.8	6.3	15.3
P_D	16.8	15.2	14.7	16.6
Γ	0.559	0.653	0.392	0.652



(a)



(b)



(c)

Figure 4. Rectification of RF causing output state changes; (a) Induced input voltage is below threshold voltage; no state changes observed at the output; (b) Induced input voltage is right around threshold voltage and RFI induced noise causes the output to change back and forth; (c) Induced input voltage is above threshold voltage; single change at the output is observed

The circuit exhibits output state changes when a relatively small amount of RF is injected. This is due to the rectification of the RF caused by the junction of the diode in the ESD protection circuit [4, 6]. The ESD rectification induces DC voltages on the P-N junctions. If this induced DC voltage is higher than the threshold voltage of the input circuit, injected RFI is interpreted as a valid signal and causes a state change at the outputs.

Fig. 4 shows the waveforms of the envelope of the RFI and the induced DC voltage at the input. As shown in Fig. 4(a), when the induced DC voltage is below the threshold voltage of the circuit, there is not enough voltage to trigger the output to make a state change. In Fig. 4(b), we increased the RFI level so that the induced DC voltage at the input pin is close to the threshold voltage. When the induced DC voltage is around the threshold voltage, the noises that are induced from the input RF envelope play a major role in the switching activities of the output. These noise spikes cross the top of the input, triggering the circuit output to switch back and forth. This means that the circuit is very sensitive to noise around the threshold voltage. In Fig. 4(c), we increased the RFI level a little bit more so that the induced DC voltage is higher than the threshold level; it is interpreted as a valid signal, causing the output to switch once per RF pulse.

IV. CONCLUSION AND FUTURE WORK

In this study we have shown that relatively low levels of pulse-modulated RFI signal can affect the normal functioning of a simple digital counter circuit by pin direct injection method to the clock network. More experiments will be done to further investigate other parameters, such as RF pulse width, pulse rise/fall time and input bias voltage's effects on the power level required to make state changes at the output. Additionally, we plan to test the susceptibility levels of data input/output and power/ground networks as compared to the clock network. Since we were limited to the frequency range of 1-1.3 GHz due to equipment limitations in this study, we are planning to test the chip over a wider frequency ranges using higher power amplifiers in the future.

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